

Tailoring etch directionality in a deep reactive ion etching tool

A. A. Ayón^{a)} and S. Nagle

*Microsystems Technology Laboratories, Massachusetts Institute of Technology,
Cambridge, Massachusetts 02319*

L. Fréchet and A. Epstein

Gas Turbine Laboratory, Massachusetts Institute of Technology, Cambridge, Massachusetts 02319

M. A. Schmidt

*Microsystems Technology Laboratories, Massachusetts Institute of Technology,
Cambridge, Massachusetts 02319*

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Silicon deep reactive ion etching is a process that produces projected two-dimensional shapes due to the inability to control the direction of the energetic ions arriving at the surface of a wafer. The resulting etched profiles present sidewalls which are nominally 90° to the wafer surface. However, we have developed and demonstrated a new technique that allows us to control the angle that trenches make with respect to the wafer surface. This scheme exploits the charging of buried dielectric layers to achieve ion steering and thus control the direction of the etch. The measured angle variation was controlled between -32° and +32° with respect to a line orthogonal to the wafer surface. We report and describe this new technique to control etch angle. © 2000 American Vacuum Society. [S0734-211X(00)04503-0]

I. INTRODUCTION

Silicon deep reactive ion etching (DRIE) is a process that produces projected two-dimensional shapes, because ions are accelerated across the dark space from a glow discharge and arrive normal to the surface of the wafer. This process results in etch profiles with sidewalls which are nominally 90° to the surface. Some modest tailoring of the etching process is possible, and can produce trenches with sloped sidewalls as illustrated in Fig. 1. Nevertheless, the etch still proceeds normal to the surface of the wafer.

We have developed and demonstrated a new technique that allows us to control the angle of the trenches with respect to the surface of the wafer. This scheme exploits the charging¹⁻⁴ of buried dielectric layers (see Fig. 2) to achieve ion steering. By exploiting the change in the local electric field at the etching surface it is possible to modify the angle trenches make with the wafer surface (see Fig. 3). We have produced trenches at angle variations as large as $\pm 32^\circ$, measured from a line orthogonal to the surface of a wafer.

II. PROCESSING APPROACH

Throughout this exercise we used 4 in., single crystal silicon wafers $\langle 100 \rangle$ of resistivity 10–20 Ω cm. This new technique involves two wafers, and it is also a two-mask process. The top wafers were double polished, 300 μ m thick, while the thickness of the bottom wafers was 525 μ m with the same resistivity values.

The first mask is used to pattern openings in a dielectric film on the bottom wafer [Fig. 4(a)]. In this experiment the thickness of the dielectric layer was chosen to be 1 μ m for silicon dioxide films, or 5 μ m for layers of photoresist

AZ4620. Independently, the top silicon wafer is spin-coated with photoresist, patterned using the second mask and etched-through. Subsequently, both wafers are aligned and either reversibly bonded using photoresist or permanently bonded [see Fig. 4(b)]. The patterned dielectric film on the bottom wafer, now covered or buried by the top wafer, is subsequently exploited to achieve ion steering.

Another possibility is to pattern the dielectric and then do a permanent silicon-to-oxide bond^{5,6} between the bottom wafer and an unprocessed top wafer as shown in Fig. 4(b). In this approach, the top wafer is structurally part of the design. For this purpose, the buried dielectric is required to be either thermal oxide or polished plasma enhanced chemical vapor deposited (PECVD) oxide, and the top silicon wafer must be double-side polished. After the bonding step has been completed, photoresist is spun on the top wafer and patterned, followed by a deep reactive ion etch (DRIE) through the top wafer, which reaches the buried dielectric and continues at an angle in the bottom wafer until a prescribed timed-etch is achieved [Fig. 4(d)]. Alignment of this masking layer can be performed by a variety of front-to-back alignment schemes. A variation would involve the use of a silicon dioxide film on the top wafer to be patterned with the photoresist mask and then used it as the DRIE mask to do the through etch. Oxide masks are etched more slowly than the photoresist masks.

Alternatively, the top wafer can be etched-through first and after stripping the photoresist it can be used repeatedly to create angle trenches by thermally oxidizing it and then performing reversible mechanical bonds with the bottom wafer. Similar to the previous paragraph, the top wafer should be double side polished. Therefore, upon completion of the etch-through and thermal oxidation steps on the top wafer its surfaces exhibit mirror-quality characteristics, which are re-

^{a)}American Vacuum Society Active Member; electronic mail: ayon@mtl.mit.edu

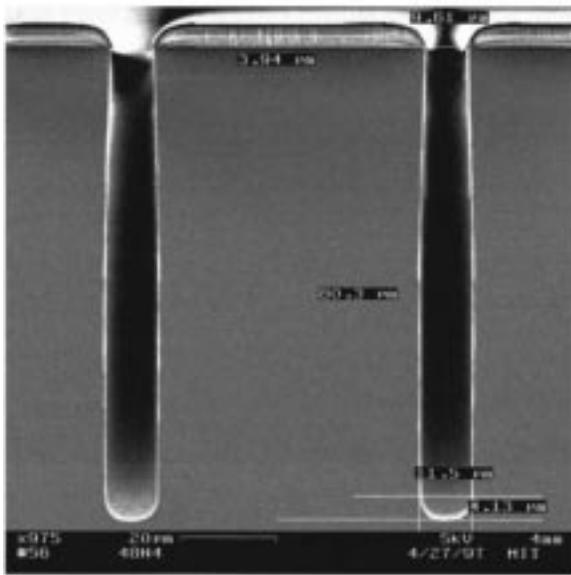


FIG. 1. During etching it is possible to tailor the profile of etched features. However, etching remains a projection of a two-dimensional shape.

quired for bonding. After preparing the surfaces of both wafers with a standard RCA clean,⁷ the samples are brought into contact and pressed together in a wafer bonder. In all operations that required aligned wafer bonding we used equipment from Electronic Visions⁸ that has been described elsewhere.⁹ After pressing the samples, an anneal step on a

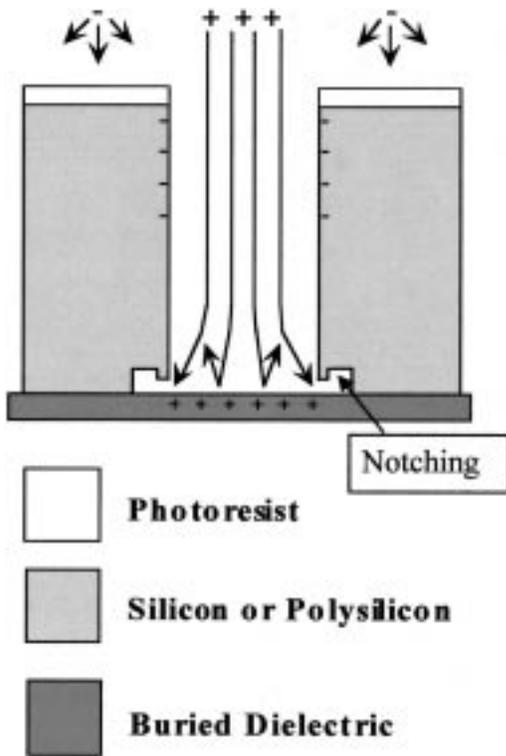


FIG. 2. When etching a silicon or polysilicon film on top of a dielectric layer, the charging of the dielectric causes the etching to continue along the interface between both layers.

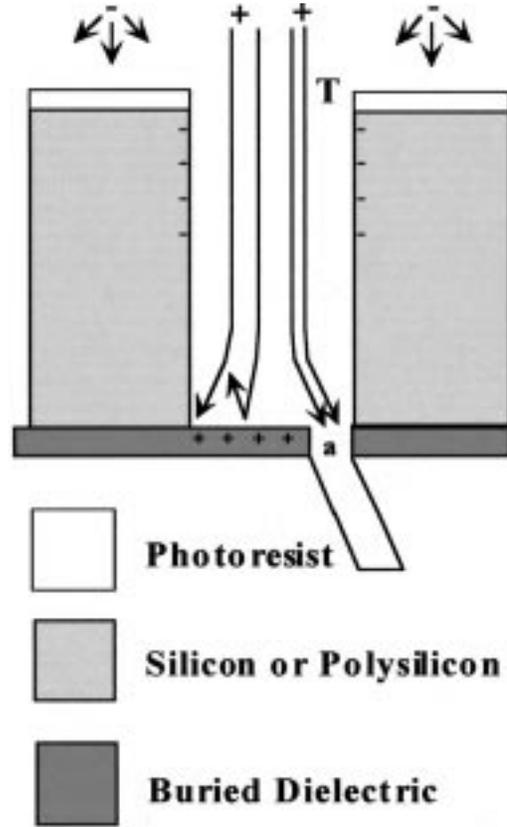


FIG. 3. Charging of the buried dielectric film allows the etching to proceed at an angle. The position of the opening *a* respect to the trench *T* on the top wafer determines the direction the etch will follow.

hot plate at a temperature of 120 °C for 10 min is usually enough to maintain the wafers in contact during processing. Upon completion of the angled-trench etching, the samples can be separated by inserting a razor blade between them.

In all cases, it is the charging of the dielectric at the interface between the two wafers that provides the electric field required for ion steering (see Fig. 5). The position of the opening in the buried dielectric (identified as *a* in Fig. 3), with respect to the opening in the top silicon wafer (identified as *T* in Fig. 3), determines the direction the trench will follow. For any particular combination of the widths *a* and *T*, the direction of the angled-trench varies from 0° when the bottom opening *a* is centered with respect to the opening *T* in the top wafer, to a maximum angle obtained when the opening *a* in the buried dielectric is located directly under the wall of the opening *T* in the upper wafer trench. Both extreme cases are shown in Fig. 5. The expectation was that it would be feasible to demonstrate a continuous variation in the angle that trenches make by varying the position of the openings in the buried dielectric with respect to the opening in the top wafer. To verify this assertion, two masks were prepared varying the width of both openings and also the position of the opening in the buried dielectric. Scanning electron microscopy (SEM) micrographs corroborating the variation of angled-etches are shown in Fig. 6.

In Fig. 6(a) the measured widths of the top and bottom

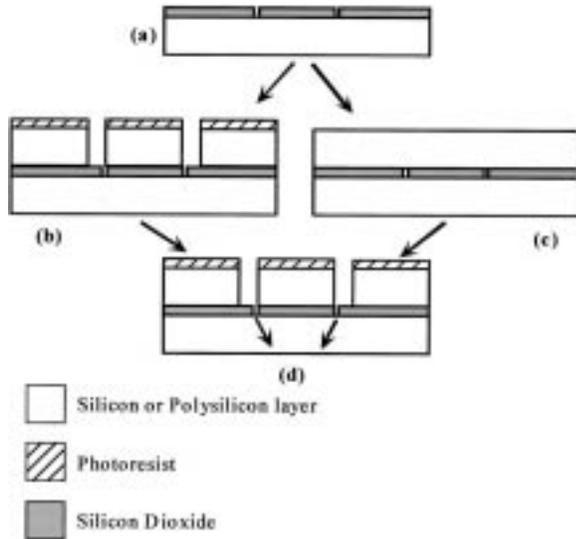


FIG. 4. General sequence scheme. (a) pattern the dielectric on the bottom wafer and then bond this sample to the top wafer. The top wafer can be prepatterned as portrayed in (b) or it can be a blank silicon wafer as shown in (c). Notice that the bond of the top/bottom pair can be permanent or reversible. (d) Charging permits tailoring the angle of the etch.

openings after etching were 19.6 and 9 μm , respectively, corresponding to a width ratio of ~ 2.2 ; the measured maximum angle was 32° . Aspect ratio can be defined as the ratio of the depth of a particular trench to the width at the top of the same trench. In the case of Fig. 6(a), the aspect ratio of the trench in the top wafer is ~ 15 . This number is relevant because it is known that smaller aspect ratios correspond to smaller charging effects,¹⁰ with the concomitant reduction in ion flux steering.

Increasing the width of the bottom opening a permits the capture of a larger ion flux. This larger ion flux can be described by a wider angular distribution function for the impinging ions compared to a bottom opening of smaller width. Since the direction of the angled-trench is controlled by the average of the ion angular distribution function, for a fixed width T , increases in the width a decrease the range of angles that the trenches can follow. This situation is exhibited in Fig. 6(b). In this SEM micrograph, the measured widths of

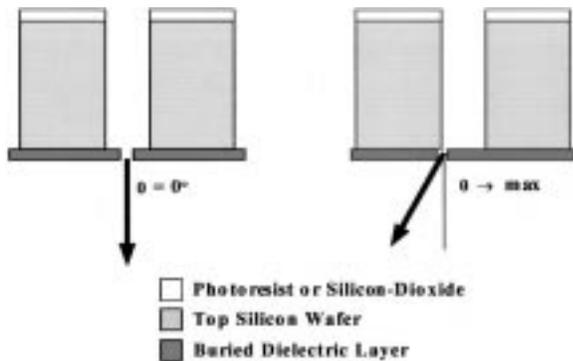


FIG. 5. Position of the opening in the buried dielectric respect to the opening in the top wafer determines the direction the etch will follow.

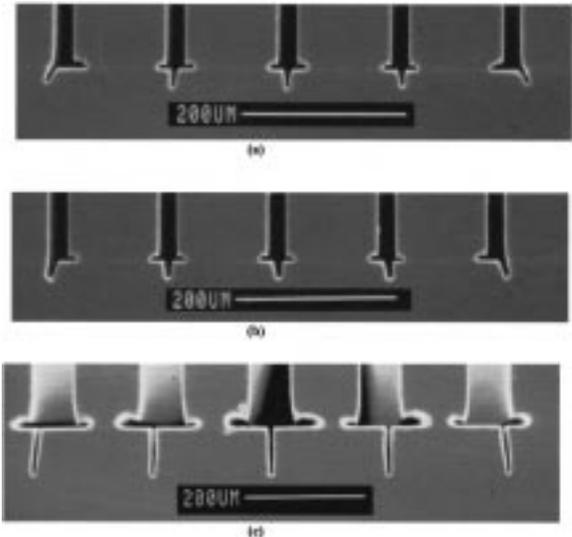


FIG. 6. Position of the opening in the buried dielectric respect to the opening in the silicon opening on top determines the ultimate direction the trench follows in the bottom silicon substrate. The footing or notching effect is clearly distinguishable on the top wafer.

the top and bottom openings after etching were of 19.3 and 11 μm respectively, representing a width ratio of ~ 1.8 and for which the measured maximum angle was 21° . Thus, the maximum angle obtained is lower than that for a width ratio of ~ 2.2 for the same trench aspect ratio in the top wafer (~ 15).

Modifying the aspect ratio of the trench in the top wafer also has a strong influence in the range of directions obtained when fabricating angled-etches. This is shown in Fig. 6(c). In this case the measured width of the trench in the top wafer was 68 μm representing a trench aspect ratio of only ~ 4.4 . The measured width of the bottom opening was 5.4, therefore, the width ratio of the top and bottom openings is ~ 12.6 . The low aspect ratio of the trench in the top wafer (~ 4.4) precludes the significant charging effect observed in those cases corresponding to pictures of Figs. 6(a) and 6(b). Thus, the direction obtained for the angled-trench close to the top wafer trench walls is only 7° .

The previous paragraphs obviate that precise alignment is necessary to obtain accurate results (see Fig. 7). Observations indicate that the process, as described herein, is reproducible within 3° .

The footing or notching^{1,4,10} effect clearly distinguishable in all SEM micrographs and that develops on the top wafer, is not an adverse artifact in this approach because the top wafer is usually only used as a mask and is subsequently removed. If the top wafer is structurally part of the final device, then the impact of the footing effect has to be assessed.

The technique described herein can be applied to previously etched wafers to add oblique etches (see Fig. 8); or it can be combined *in situ* with ordinary trenches etched normal to the surface of the wafer.

The demonstration was made using high-density plasma; inductively coupled DRIE tool from surface technology

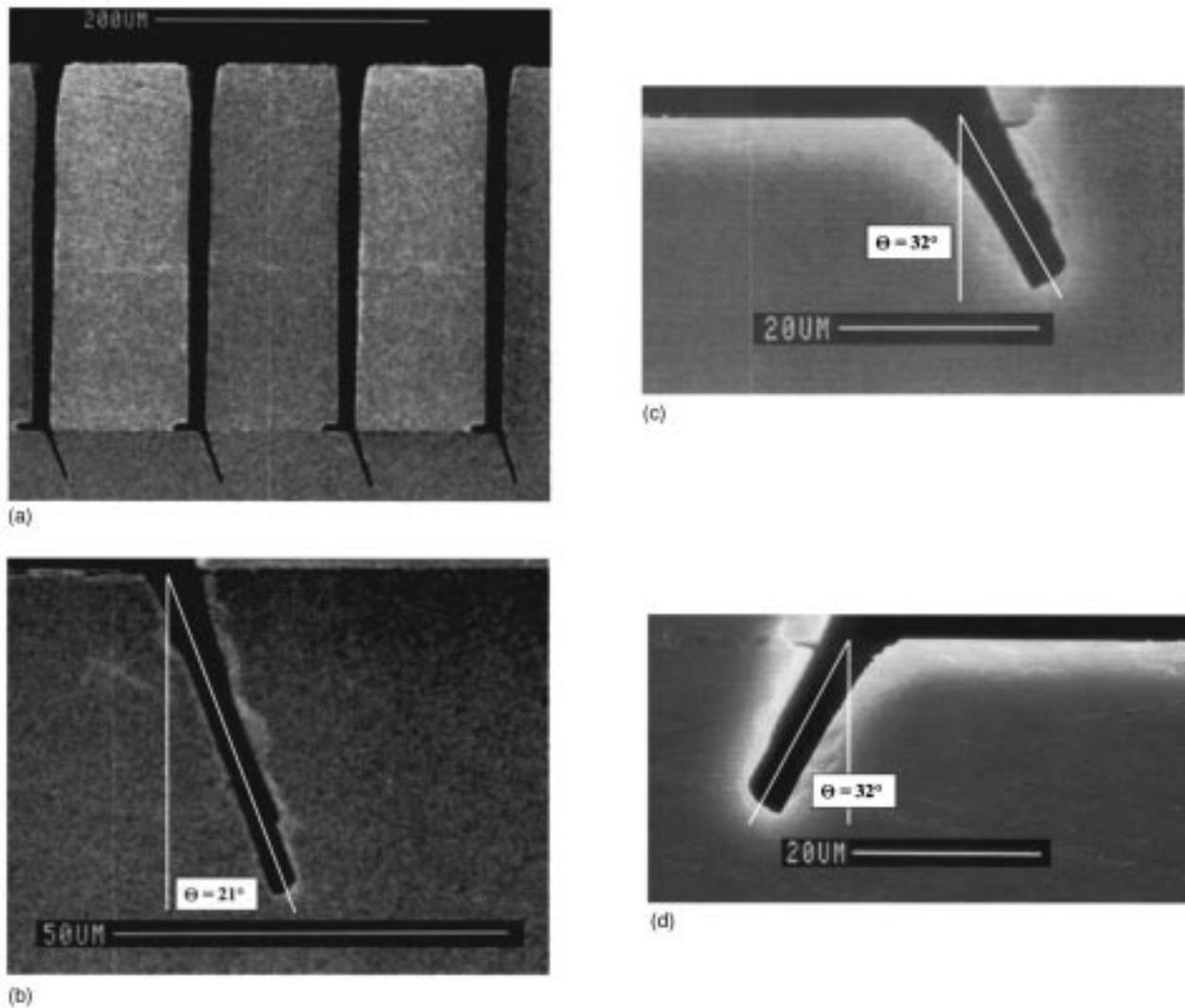


FIG. 7. SEM micrographs in (a) and (b) show an array of trenches making an angle of 25° with respect to a line normal to the surface of the wafer, and a close-up of one of those trenches. (c) and (d) are SEM micrographs of trenches making an angle of 32° respect to the normal to the surface of the wafer.

systems¹¹ that has been described elsewhere.^{12–14} The operating conditions were chosen as follows: during the etching cycle the SF_6 flow rate was fixed at 105 sccm, with a cycle duration of 14 s, 12 W of applied electrode power, and 750 W of applied coil power. The overlap between the etch step and the passivating step was 0.5 s. During the passivation cycle the C_4F_8 flow rate was fixed at 40 sccm, with a cycle duration of 11 s, 6 W of applied electrode power, and 600 W of applied coil power. The throttle valve was positioned throughout the process at 65° .

Under the above conditions the described technique displays the characteristic high silicon etching rate ($\sim 3 \mu\text{m}/\text{min}$) and high selectivity to masking material ($\geq 70:1$ for photoresist, $\geq 140:1$ for silicon dioxide) commonly ascribed to DRIE tools when etching the top wafer.⁹ However, upon reaching the opening in the buried dielectric (identified as a in Fig. 3), whose width is smaller than the opening in the top wafer (identified as T in Fig. 3), the captured ion flux available to proceed with the angle etch is proportional to the

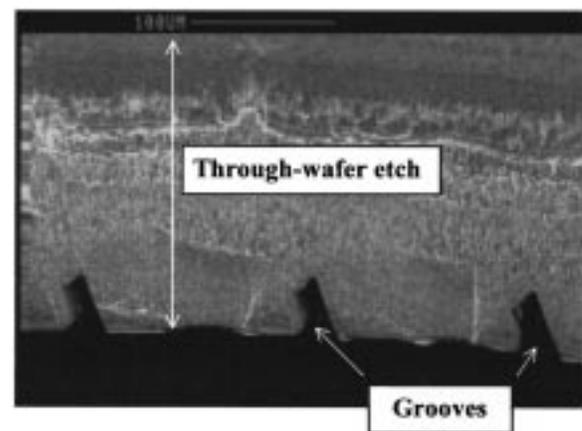


FIG. 8. Technique presented in this manuscript permits the etching of cuts or grooves at an angle on samples that have already undergone previous etches.

fraction a/T of the total ion flux reaching the interface between both wafers. Thus, the etching rate of the angle trench is similar to that of a trench of width a and whose depth is the thickness of the top wafer.

III. CONCLUSIONS

This technique overcomes well-known shortcomings of other approaches. For instance, chemical assisted ion beam etching^{15–18} (CAIBE) has the ability of producing trenches at any angle; however it requires a dedicated piece of equipment and each angle selected requires a different etch preceded by the corresponding photolithography steps. In comparison, the technique described herein allows the etching of trenches in any direction simultaneously, by exploiting the charging of a buried dielectric layer when using high-density plasma DRIE machines.

We believe that this technique can be useful in a large variety of microelectromechanical systems (MEMS) devices, which employ DRIE. For instance, in microfluidic applications arrays of channels with the proper angle distributions can be used to produce swirl. Cones can be microfabricated for check valve applications. Fluid channels converging in a point for mixing can be produced with the additional degree of freedom presented in this manuscript. Microrotating machinery may also benefit by the production of airfoils that more closely resemble their macroscale counterparts by exhibiting a 3D twist. The ability to control the angle of an etch can enable the fabrication of grooved journal bearings as pictured in Fig. 8. This SEM micrograph shows a fabricated device that is one step closer to producing spiral-grooved journal bearings also known as Herringbone bearings.¹⁹

In summary, the scheme for etching silicon trenches at an angle contained herein, complements current microfabrication technologies, expands our ability to tailor the shape of microfabricated structures, and reduces a significant design constraint.

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