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THICK BURIED OXIDE IN SILICON (TBOS): AN INTEGRATED FABRICATION TECHNOLOGY FOR MULTI-STACK WAFER-BONDED MEMS PROCESSES

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ABSTRACT

This paper reports on work to develop an integrated fabrication technology called TBOS that enables the use of thick PECVD oxide films (10 to 20 μm thick) within a multi-stack wafer bonded device. The development of TBOS is driven by a need to integrate a two-level interconnect device into a five-level-stack wafer-bonded MEMS microstructure. The PECVD oxide films are characterized and shown to induce a large wafer bow of up to 230 μm for a layer of 10 μm thick, and exhibit cracks for thicknesses greater than 15 μm after the densification process at 1100°C in N_2 ambient. A combination of CMP and timed field-etching processes are used to form isolated regions of thick PECVD oxide buried in a planar surface. This microfabrication approach reduces the wafer bow by at least 50% and allows insulating layers without cracks, hence enabling the development of the high voltage Power MEMS devices.

Keywords: TBOS, PECVD Oxide, CMP, Multi-level Interconnects, Wafer Bonding.

INTRODUCTION

The integration of Thick Buried Oxide in Silicon (TBOS) with micromachined structures enables the development of high power density micro-devices with considerable improvements in performance and efficiency. TBOS is a process technology that provides integration of thick, planarized and bondable plasma-enhanced chemical-vapor deposited (PECVD) oxide films, in the range of 10 to 20 μm thick, within a multi-stack wafer-bonded device. It provides localized thick oxide regions with planarized surfaces using chemical mechanical polishing (CMP) allowing their integration within a MEMS device. The localized oxide regions then become the base insulation for thin film processes that can ultimately be etched and bonded with other wafers. This paper presents challenges and solutions for the use of TBOS in the development of MEMS-based micro-devices that uses aligned multi-stack wafer-bonded processes. The critical process issues are (1) fracture, which limits oxide thickness, and (2) stress, which creates wafer bow that interferes with wafer bonding.

PROCESS TECHNOLOGY DEVELOPMENT

The effort to develop TBOS is motivated by the integration of high voltage micro-motors within micro-turbomachinery-based Power MEMS [1]. The fabrication design requires a process flow for electrical components consisting of rotating and stationary structures, a rotor and a stator, that would allow their integration into a five-wafer bonded silicon microstructure [2]. The high power requirement involves high voltages, which leads to the use of thick oxide films in order to reduce capacitive loading. Localized thick oxide regions are constructed to insulate the electrical components from the bulk silicon substrate while providing planarized thin oxide fields for the formation of fluidic channels by way of deep etches into the silicon substrate. Figure 1 shows a schematic of a micro-motor driven compressor that uses this fabrication method. In this process, for example, TBOS allows the insulation of a weakly conducting polysilicon rotor film and two-level polysilicon stator electrodes and interconnects from the silicon substrates. The stator fabrication flow integrates a two-level polysilicon interconnect process with MEMS fabrication technologies such as deep reactive ion etching and aligned wafer level bonding. This multilevel interconnect process must lead to a planar, unbowed surface to allow bonding to the silicon structure and maintain a 3 μm gap between the rotor and stator. The two - level polysilicon stator

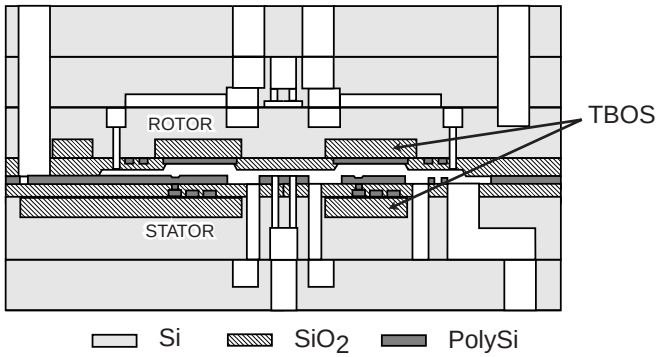


Figure 1 - Schematic of a micro-motor driven compressor that uses TBOS to insulate the rotor and stator electrical components from the silicon substrates.

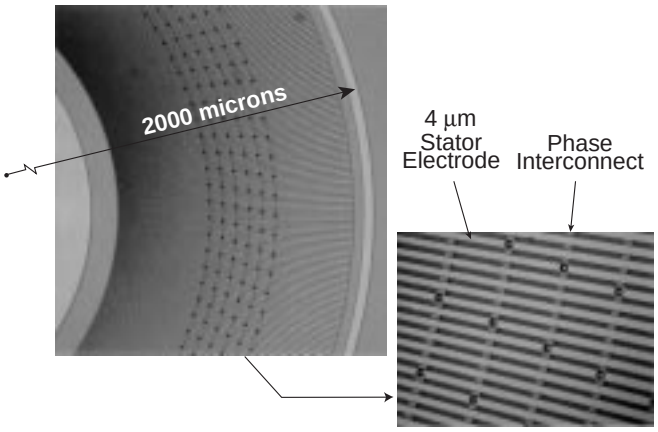


Figure 2 - Optical micrographs of a two-level polysilicon stator structure that gets insulated from the silicon substrate by using TBOS.

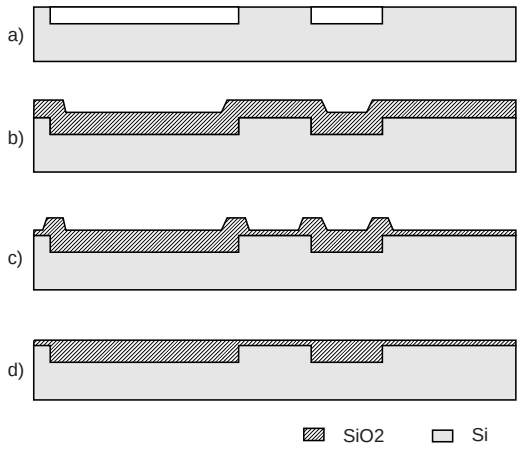


Figure 3 - TBOS process consists of (a) silicon dry etching, (b) thick PECVD oxide deposition, (c) timed-field oxide etching, and (d) CMP process steps.

process joins 786 electrodes into 6 phases that are separated by a planarized inter-level dielectric. Figure 2 shows optical micrographs of a stator structure. This paper focuses on the characterization processes needed to develop TBOS for applications requiring integration, such as the two-level polysilicon stator component in a micro-motor driven compressor device.

TBOS Process

The TBOS process for high voltage micro-motor electrical components consists of 10 μm thick PECVD oxide films deposited over wide silicon trenches (Figure 3). A combination of timed-field oxide etching and CMP of 10 μm high ridges provides a planarized surface containing recessed oxide islands.

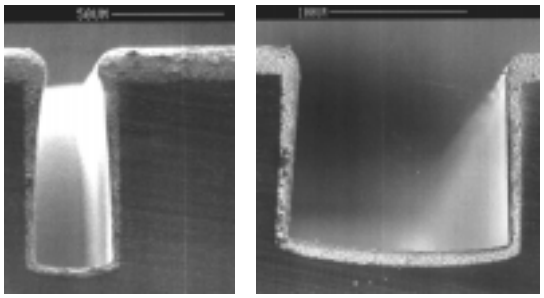
The development for TBOS was started by fabricating 10 μm deep, 4 mm wide silicon trenches with flat bottom surfaces (less than 0.5 μm bow) using an etch recipe in a plasma system (Applied Materials AME5000) with Cl_2 and HBR gases (Figure 3a). A layer of 12 μm thick PECVD oxide film is deposited on the wafer (system described in the next section) and then densified at 1100°C in N_2 ambient (Figure 3b). The sample was coated with a 10 μm thick AZ4620 photoresist and patterned with a contact aligner with a wavelength of 320 nm and power density of 6 mW/cm^2. The patterned photoresist covered the filled oxide regions and it was offset by 100 μm. The sample was then timed-etched in a BOE solution of 7:1 concentration to remove the 10 μm oxide in the field region with an etch rate of approximately 1000 Å/min, followed by a piranha clean (H_2SO4: H_2O_2 4:1) to remove the photoresist. This resulted in 10 μm high, 100 μm wide bumps on the periphery of each buried oxide region (Figure 3c) which was planarized using CMP (Figure 3d).

This process results in reduced wafer bow and eases deep reactive ion etching in the field regions. Without this approach, the 10 μm thick PECVD oxide films exhibit an induced compressive film stress of up to 210 MPa and a wafer bow of up to 230 μm that could result in difficulties during the aligned multi-stack wafer bonding. In order to use TBOS effectively we needed to understand the fundamental fabrication challenges and limitations such as deposition and characterization of the thick PECVD oxide films and their surface uniformity and planarization using CMP.

Deposition and Characterization

In this process, the PECVD oxide films are deposited using a five-station continuous plasma processing system (Concept One, Novellus Inc.) [3]. The film deposition conditions involve flows of 300 sccm of SiH_4, 9500 sccm of N_2O and 1500 sccm of N_2. The oxide deposition is performed at low temperature (400°C) with deposition rates of the order of 1 μm/min. The wafer-level oxide thickness has a nonuniformity better than 1% and a nominal residual stress between 50 and 80 MPa.

The hydrogen content of these films is less than 8% as measured with Rutherford back-scattering spectroscopy with accelerated doubly ionized helium atoms (He^{++}) incident on the sample surface. Because of its deleterious effects on the electrical characteristics of deposited films [4,5], it is advantageous to remove the hydrogen. This step is achieved by densifying the film immediately after deposition. Densification is accomplished by subjecting the films to a temperature of 1100°C for one hour while a steady N_2 flow is maintained in the furnace. After densification, the measured hydrogen content falls below 0.2%.



(a) *(b)*

Figure 4 – PECVD oxide films are characterized by their lack of conformality, which is worse for high aspect ratio trenches (a) when compared to low aspect ratio trenches (b).

The films are also characterized for their non-conformality. It was found that deposition of thick oxide films with good conformality is achievable in low aspect ratio trenches. Figures 4 a&b show silicon trenches of 80 μm deep, 40 μm wide and 130 μm deep, 170 μm wide with deposited layers of 16 μm and 20 μm thick PECVD oxide films, respectively. Figure 4a shows a key-hole effect, that can be problematic in high aspect ratio trenches because of the observed sealing at the top of the etched features. This effect is however not critical for the low aspect ratio trenches involved in this demonstration, as can be observed in Figure 4b.

The wafer-level film thickness nonuniformity is monitored. The Concept One is capable of depositing PECVD oxide films with an averaging effect that results in high throughput, uniformity and repeatability [3]. Using an optical interferometric system, Tencor SM300, the measured wafer-level oxide thickness nonuniformity, deposited over a 4" single polished silicon wafer, is less than 1%. This measurement is made routinely at five separate points across the wafer for thicknesses in the range of 1–10 μm. There is, however, a 3% thickness reduction in the oxide film across the wafer after it is densified at 1100°C for one hour in N_2 ambient.

The use of thick oxide films in MEMS devices requires an understanding of the inherent physical properties, such as residual stress and wafer bow, that are associated with any thick films. Using our general deposition recipe for PECVD oxide, the deposited films greater than 15 μm in thickness have exhibited cracks during densification at 1100°C at a steady N_2 flow. Figure 5 shows a SEM cross section of a 20 μm thick oxide film that exhibits cracking.

The residual stress and wafer bow are measured for a matrix of 1, 2, 5 and 10 μm thick PECVD oxide films. Using a thin film stress measurement instrument,

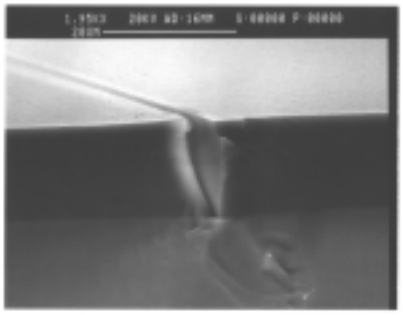


Figure 5 – SEM showing a crack which develops in a 20 μm thick deposited oxide layer after densification at 1100°C.

Tencor FLX-2320, the changes in the radius of curvature of the silicon substrate caused by the deposition of the film was measured and calculated automatically based on the Stoney Formula [6]. We made a total of three separate measurements for each film thickness before and after densification at 1100°C. The average measured compressive stress for all five different thicknesses were between 50 MPa and 200 MPa for the undensified and densified PECVD oxide films, respectively. These data indicate that the induced film stress is independent of thickness. The wafer bow is approximately proportional to the film thickness and it is at least a factor of four larger for densified films than undensified ones. Figure 6 shows a graph of the measured wafer bow versus film thickness for both undensified and densified films. The average wafer bow for three TBOS wafers was measured to be 55 μm. The TBOS process therefore reduces the wafer bow by approximately five times compared to a uniform 12 μm film.

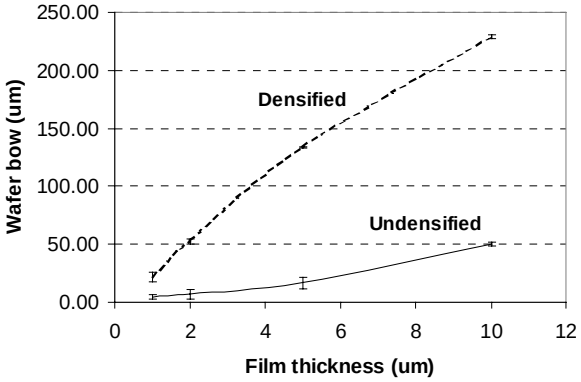


Figure 6 – A graph showing measured wafer bow for undensified and densified 1-10 μm thick PECVD oxide films. Each point is an average of three separate measurements for each thickness.

Surface Planarization

In recent years, CMP has become a primary technique for planarizing inter-level dielectrics (ILD) and metal layers for sub-micron VLSI fabrication, and lately for direct wafer bonding [7]. CMP is used in this project as a key process to develop TBOS by achieving: 1) flat, planarized and localized oxide islands with reduced wafer bow, and 2) enhanced surface smoothness on the PECVD oxide films. These two issues allow direct wafer bonding in a multi-stack MEMS structure.

The planarization of the 10 μm high, 100 μm wide PECVD oxide bumps for the TBOS process was carried out to achieve maximum flatness of the buried oxide regions without sacrificing the uniformity of the oxide film in the field region. The sample was polished on a Strasbaugh 6EC Laboratory Planarizer with the IC-1400 polishing pad and the ammonium based Semi-Sperse 25 Slurry. Prior to each run, the removal rate was first determined on a 1 μm thick densified PECVD oxide film, deposited on a flat silicon wafer. The polishing time was then adjusted to remove the 10 μm thick oxide bumps. For an optimized CMP polishing condition of 4 psi down force, carrier speed of 25 rpm and table speed of 15 rpm, the average oxide removal rate was 16 Å/s for the densified 1 μm thick flat oxide and 150 Å/s for the densified 10 μm high, 100 μm wide bumps. The uniformity of the polished film on the bumps versus field was determined largely by the down force pressure and the length of polishing time. The results indicate a 4000 Å wafer-level oxide thickness nonuniformity on the field region and an average of 0.6 μm thickness variation between the field and the center of each die. The other aspect of planarization that influences bonding is surface smoothness. Using an atomic force microscopy (AFM), the measured root mean square roughness of a 1 μm thick densified PECVD oxide film was measured to be 9 nm. This value was dropped by a factor of 22 to 0.4 nm after the sample was polished for 60 seconds using the same CMP recipe as described above. The polished sample was then fusion bonded successfully with an identical polished 1 μm thick densified PECVD oxide film, a low stress silicon nitride and a single polished silicon wafer.

DISCUSSION

A study is underway to optimize the current existing TBOS process by accurately monitoring and improving the flatness of the 10 μm deep silicon trenches as well as planarizing the 10 μm thick oxide bumps with respect to the field region. The latest CMP characterization results show that multi-step oxide deposition of up to 26 μm thick is possible if the densification is postponed until the isolated oxide islands are formed. This modification prevents cracks on the thick oxide regions and limits its deposition area.

CONCLUSION

The characterization of thick PECVD oxide films that functioned both as a dielectric and as an isolation layer were demonstrated. We have developed TBOS as an engineering solution to overcome the inherent physical problems such as wafer bow and cracks in the thick oxide films for applications that require a combination of CMOS and MEMS based processes. More importantly, the preliminary results show that wafer-level integration can be realized by wafer bonding of planarized thick PECVD oxide surfaces but yet have to be demonstrated in a 5-layer bonded stack.

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REFERENCES

[1] A. H. Epstein et al., " Power MEMS and Microengines", *Transducers '97*, Vol. 2, 1997, pp. 753- 756

[2] C-C Lin, R. Ghodssi, A. A. Ayon, D-Z Chen, S. Jacobson, K. Breuer, A. H. Epstein and M. A. Schmidt, "Fabrication and Characterization of a Micro Turbine/Bearing Rig", *IEEE MicroElectroMechanical Systems '99*, Orlando, Fl, 1999, pp. 529-533

[3] *Novellus Systems Inc.*, 81 Vista Montana, San Jose, CA 95134

[4] S. P. Murarka, S. C. Li, X. S. Guo and W. A. Lanford, "The Capacitance-Voltage Characteristics and Hydrogen Concentration in Phospho-Silicate Glass Films: Relation to Phosphorous Concentration and Annealing Effects," *J. Appl. Phys.*, Vol. 72, No. 9, pp. 4208-4213, 1992

[5] M. G. J. Veprek-Heijman and D. Boutard, "The Hydrogen Content and Properties of SiO2 Films Deposited from Tetraethoxysilane at 27 MHz in Various Gas Mixtures," *J. Electrochem Soc.*, Vol. 138, No. 7, pp. 2042-2046, 1991

[6] User Manual to Tencor FLX-2320, *Tencor Inc.*, 2400 Charleston Road, Mountain View, CA 94043

[7] C. Gui, M. Elwenspoek, J. G. E. Gardeniers and P. V. Lambeck, "Present and Future Role of Chemical Mechanical Polishing in Wafer Bonding," *J. Electrochem Soc.*, Vol. 145, No. 6, pp. 2198-2204, 1998